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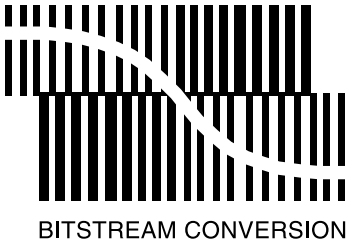
DATA SHEET



UDA1360TS
Low-voltage low-power stereo audio ADC

Preliminary specification
Supersedes data of 1998 Oct 02
File under Integrated Circuits, IC01

2000 Feb 08

Philips Semiconductors

PHILIPS

Low-voltage low-power stereo audio ADC UDA1360TS

FEATURES

General

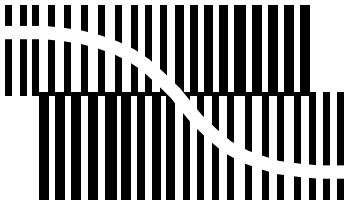
- Low power consumption
- 2.4 to 3.6 V power supply
- Supports 256 and 384f_s system clock
- Supports sampling frequency range of 5 to 55 kHz
- Small package size (SSOP16)
- Integrated high-pass filter to cancel DC offset
- Power-down mode
- Supports 2 V (RMS) input signals
- Easy application
- Non-inverting ADC plus decimation filter.

Multiple format output interface

- I^2S-bus and MSB-justified format compatible
- Up to 20 significant bits serial output.

Advanced audio configuration

- Stereo single-ended input configuration
- High linearity, dynamic range and low distortion.



GENERAL DESCRIPTION

The UDA1360TS is a single chip stereo Analog-to-Digital Converter (ADC) employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording functions.

The UDA1360TS supports the I^2S-bus data format and the MSB-justified data format with word lengths of up to 20 bits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I_{DDA}	analog supply current		–	9	–	mA
I_{DDD}	digital supply current		–	3.5	–	mA
T_{amb}	operating ambient temperature		–40	–	+85	°C
ADC						
$V_{i(rms)}$	input voltage (RMS value)	see Table 1	–	1.0	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–37	–33	dB
S/N	signal-to-noise ratio	V_I = 0 V; A-weighted	–	97	–	dB
α_{cs}	channel separation		–	100	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1360TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

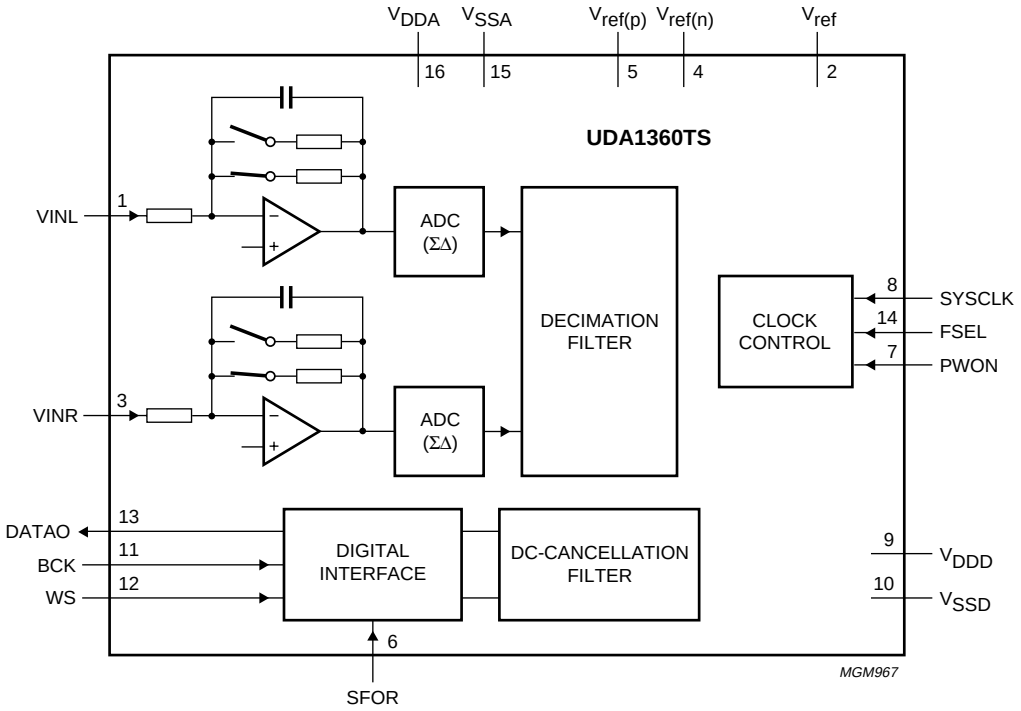


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VINL	1	left channel input
V_{ref}	2	reference voltage
VINR	3	right channel input
$V_{ref(n)}$	4	ADC negative reference voltage
$V_{ref(p)}$	5	ADC positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock input 256 or 384f_s
V_{DDD}	9	digital supply voltage
V_{SSD}	10	digital ground
BCK	11	bit clock input
WS	12	word selection input
DATAO	13	data output
FSEL	14	system clock frequency select
V_{SSA}	15	analog ground
V_{DDA}	16	analog supply voltage

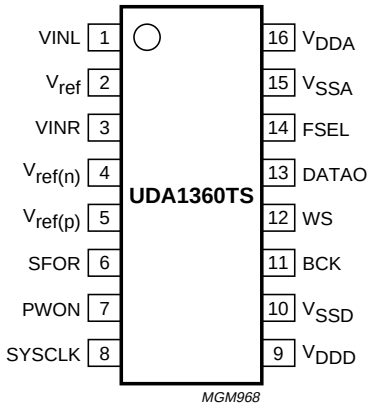


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System clock

The UDA1360TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable via the static FSEL pin, and the system clock must be locked in frequency to the digital interface input signals.

The options are 256f_s (FSEL = LOW) and 384f_s (FSEL = HIGH). The sampling frequency range is 5 to 55 kHz.

The BCK clock can be up to 128f_s, or in other words the BCK frequency is 128 times the Word Select (WS) frequency or less: $f_{BCK} \leq 128 \times f_{WS}$.

Notes:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.
2. For MSB justified formats it is important to have a WS signal with 50% duty factor.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1360TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

Input level

The overall system gain is proportional to V_{DDA}. The 0 dB input level is defined as that which gives a –1 dB FS digital output (relative to the full-scale swing). In addition, an input gain switch is incorporated with the above definitions.

The UDA1360TS front-end is equipped with a selectable 0 or 6 dB gain, in order to supports 2 V (RMS) input using a series resistor of 12 kΩ.

For the definition of the pin settings for 1 or 2 V (RMS) mode given in Table 1, it is assumed that this resistor is present as a default component.

If the 2 V (RMS) signal input is not needed, the external resistor should not be used.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Multiple format output interface

The UDA1360TS supports the following data output formats;

- I^2S-bus with data word length of up to 20 bits
- MSB-justified serial format with data word length of up to 20 bits.

The output format can be set by the static SFOR pin. When SFOR is LOW, the I^2S-bus is selected, when SFOR is set HIGH the MSB-justified format is selected.

The data formats are illustrated in Fig.4. Left and right data channel words are time multiplexed.

Decimation filter

The decimation from $128f_s$ is performed in two stages. The first stage realizes 3rd-order sin x/x characteristic. This filter decreases the sample rate by 16. The second stage (an FIR filter) consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 DC cancellation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple		none
Pass-band gain		0
Stop band	$>0.55f_s$	−60
Droop	at $0.00045f_s$	0.031
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	>110

Mute

On recovery from power-down, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time tracks with the sampling frequency:

$$t = \frac{12288}{f_s} = 279 \text{ ms ; where } f_s = 44.1 \text{ kHz.}$$

Power-down mode

The PWON pin can control the power saving together with the optional gain switch for 2 V (RMS) or 1 V (RMS) input. When the PWON pin is set LOW, the ADC is set to power-down. When PWON is set to HIGH or to half the power supply, then either 6 dB gain or 0 dB gain in the analog front-end is selected.

Application modes

The UDA1360TS can be set to different modes using two 3-level pins and one 2-level pin. The selection of modes is given in Table 3.

Table 3 Mode selection summary

PIN	V_{SS}	$\frac{1}{2}V_{DD}$	V_{DD}
SFOR	I^2S-bus	test mode	MSB
PWON	power-down	0 dB gain	6 dB gain
FSEL	$256f_s$	–	$384f_s$

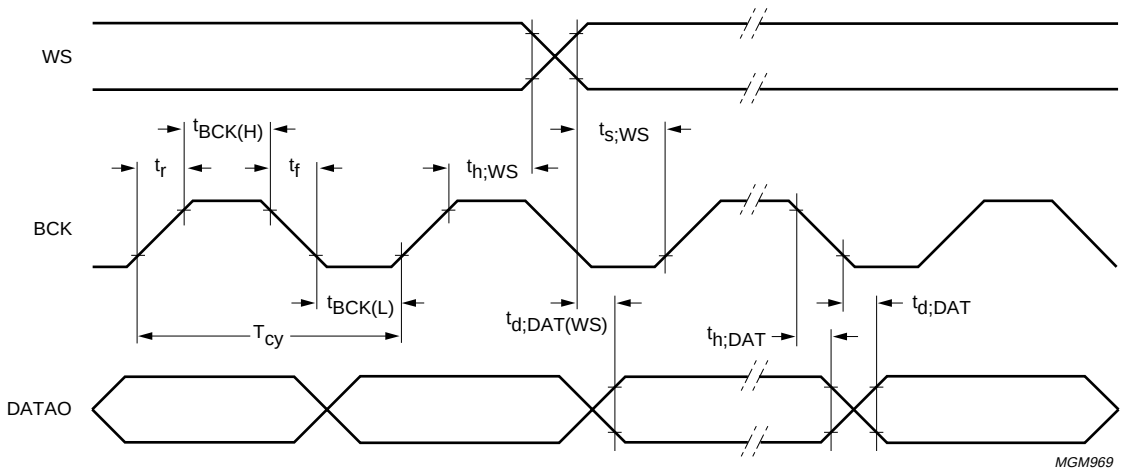


Fig.3 Serial interface timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltage referenced to ground, $V_{DDD} = V_{DDA} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
V_{DDA}	analog supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 2	–3000	+3000	V
		note 3	–300	+300	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	140	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 3$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 10 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage	note 1	2.4	3.0	3.6	V
V_{DDD}	digital supply voltage	note 1	2.4	3.0	3.6	V
I_{DDA}	analog supply current	operation mode	–	9	–	mA
		power-down mode	–	3.5	–	mA
I_{DDD}	digital supply current	operation mode	–	3.5	–	mA
		power-down mode	–	0.5	–	mA
Digital inputs						
PINS BCK, FSEL, SYSCLK AND WS						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_I	input capacitance		–	–	10	pF
PINS PWON AND SFOR						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IM}	MIDDLE-level input voltage		$0.3V_{DDD}$	–	$0.7V_{DDD}$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
Digital output; Pin DATAO						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
Analog						
V_{ref}	reference voltage	referenced to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
R_I	input resistance		–	12	–	kΩ
C_I	input capacitance		–	20	–	pF

Note

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = 3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 10 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{i(rms)}$	input voltage (RMS value)	see Table 1	1.0	–	V
ΔV_i	unbalance between channels		0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–85	–80	dB
		at –60 dB; A-weighted	–37	–33	dB
S/N	signal-to-noise ratio	$V_I = 0$ V; A-weighted	97	–	dB
α_{cs}	channel separation		100	–	dB
PSRR	power supply rejection ratio		30	–	dB

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = 2.7$ to 3.6 V; $T_{amb} = -20$ to +85 °C; all voltages referenced to ground (pins 10 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
T_{sys}	clock cycle	$f_{sys} = 256f_s$	71	89	782	ns
		$f_{sys} = 384f_s$	47	59	522	ns
t_{CWL}	f_{sys} LOW-level pulse width		$0.4T_{sys}$	–	$0.6T_{sys}$	ns
t_{CWH}	f_{sys} HIGH-level pulse width		$0.4T_{sys}$	–	$0.6T_{sys}$	ns
Serial data timing (see Fig.3)						
T_{cy}	bit clock cycle		$\frac{1}{64}f_s$	–	–	ns
$t_{BCK(H)}$	bit clock HIGH time		100	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{d;DAT}$	data output delay time (from BCK falling edge)		–	–	80	ns
$t_{d;DAT(WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	80	ns
$t_{h;DAT}$	data output hold time		0	–	–	ns
$t_{s;WS}$	word selection set-up time		20	–	–	ns

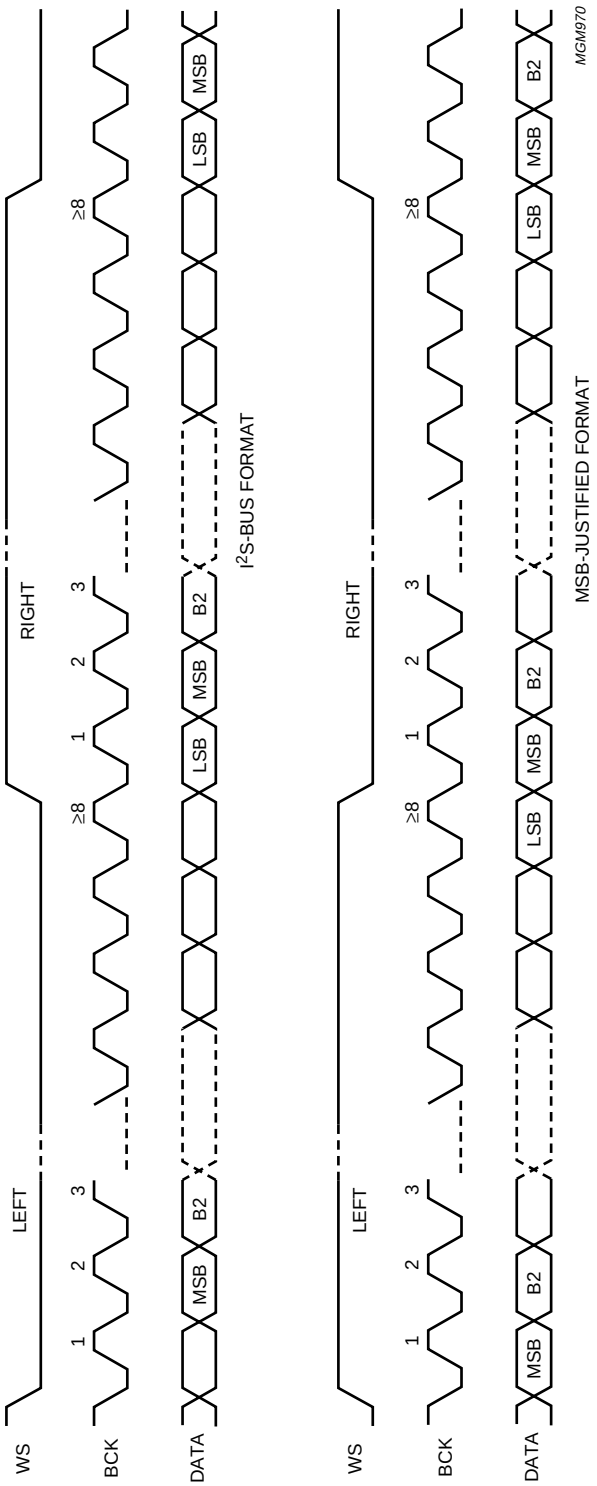


Fig.4 Serial interface formats.

APPLICATION INFORMATION

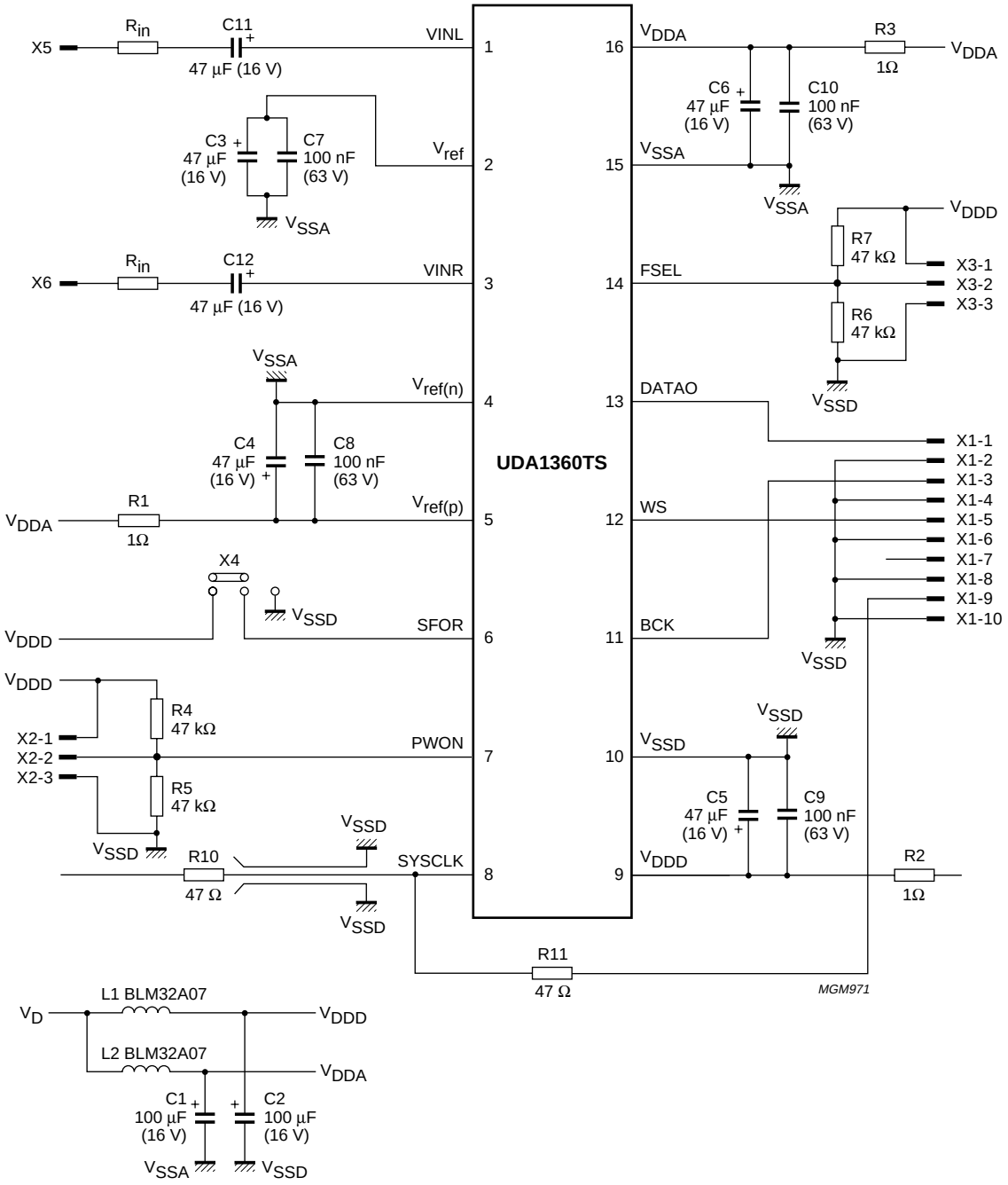
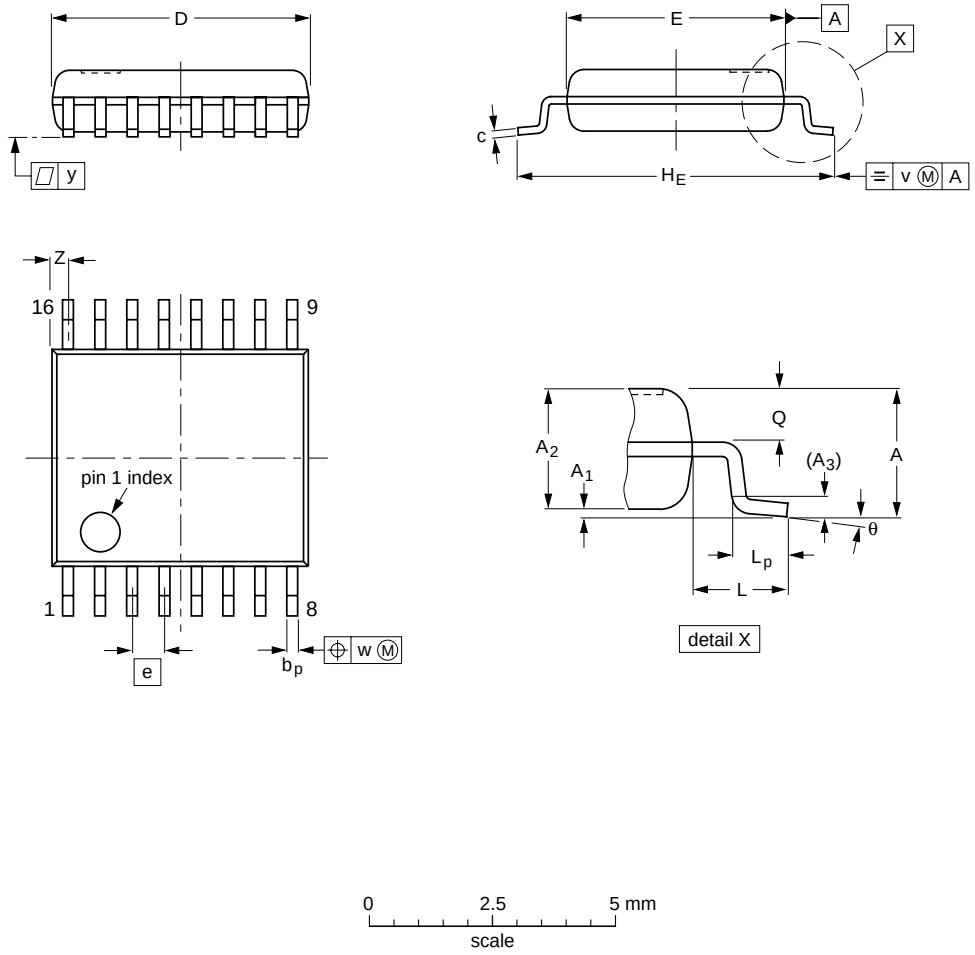


Fig.5 Application diagram.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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